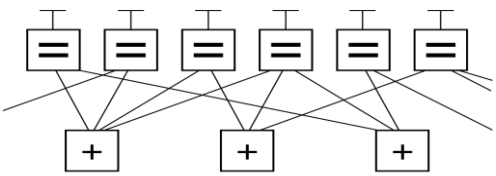
LDPC Decoder

The **LDPC Decoder** is a highly optimized IP core intended to work with Xilinx FPGAs and Vivado HLS tools. The LDPC Decoder is used in forward error correction applications to correct for errors introduced while sending data over a noisy channel. The LDPC Decoder can be delivered either as an encrypted netlist, or as synthesizable C++ source code.

Features

- Low latency, high throughput LDPC Decoder
- Up to 7464 Msps throughput for single iteration, 1508 Msps for 5 iterations
- High-Level Synthesis (C++) implementation
- Suitable for communications standards, such as:
  IEEE 802.11ac, Gigabit Ethernet
- Number of iterations from 1 – 5



Parameterization

- Z Block Parallelization (BP): 1, 3, 9
  Defines the number of LDPC processing engines (small FPGA footprint vs high throughput)
- Soft Bit Width
  Defines the width of the soft bit values

High-Level Synthesis Design

- Synthesizable C++ code for FPGAs
- Support for Xilinx Vivado HLS and 3rd party HLS tools
- allows for higher level abstraction than RTL
- Highly optimized C++ code as well as low-level optimizations (individual LUTs, memories, etc.)
- Fast validation using C/C++ testbench
- Easy integration into existing HLS or RTL projects

Timing (Max Clock Frequency)

(examples based on Kintex Ultrascale FPGAs)

Parallelism	Fmax
1	452 MHz
3	416 MHz
9	350 MHz

*Note, Fmax will depend on FPGA device, speed grade, design density and other design factors.

Throughput and Resource Utilization

(examples based on Kintex Ultrascale FPGAs)

Throughput

Parallelism	1 Iterations	5 Iterations
1	266 ~ 1211 Mbps	20 ~ 96 Mbps
3	624 ~ 2880 Msps	52 ~ 250 Mbps
9	1070 ~ 5063 Msps	109 ~ 532 Mbps

*Throughput depends on packet parameters (the number of parity blocks in the matrix, and the size of the blocks) and noise level. The LDPC decoder has been designed so that the throughput meets requirements of standards such as 802.11ac.

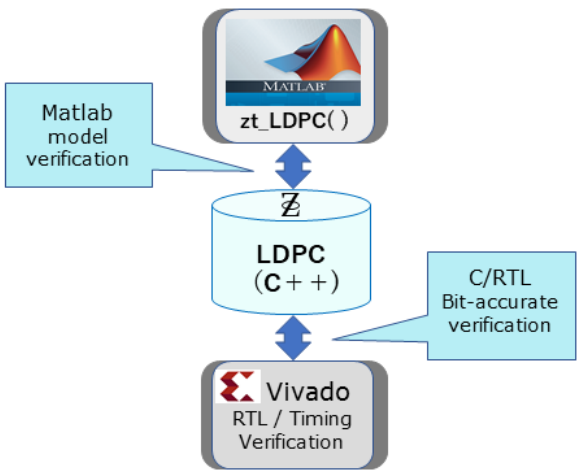
Resource Utilization

Parallelism	CLB	LUT	FF	BRAM
1	2140	11167	17240	80
3	4566	27382	38155	144
9	13257	83673	93820	360

*Resource utilization will vary depending on the target clock frequency. More pipeline registers will automatically be inserted in order to meet higher frequencies.

Testing and Verification

- Tested in C, RTL simulation and hardware
- Used by customers in a high-performance communications system
- C++ testbench included
- Verified using Matlab reference design



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