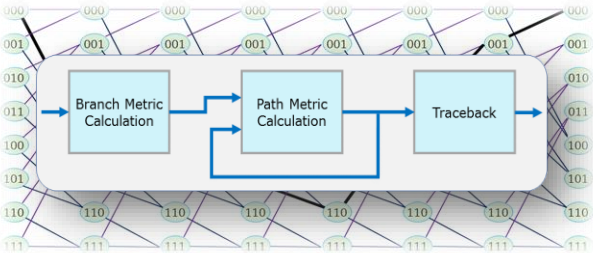
Viterbi Decoder

The **Zotech Viterbi Decoder** is a highly optimized IP core intended to work with Xilinx FPGAs and Vivado HLS tools. The Viterbi Decoder is used in forward error correction applications to correct for errors introduced while sending data over a noisy channel. The Viterbi Decoder can be delivered either as an encrypted netlist, or as synthesizable c++ source code.

Features

- Low latency, high throughput Viterbi Decoder
- Up to 722 Msps throughput
- High-Level Synthesis (C++) implementation
- Suitable for communications standards, such as:
  3GPP LTE, IEEE 802.11,
- Bit-accurate with Matlab's vitdec function



Parameterization

- Two architectures to choose from:
  2 encoded bits in -> 1 decoded bit out
  4 encoded bits in -> 2 decoded bits out
  (small FPGA footprint vs high throughput)
- Soft-bit width
- Traceback length (up to 128)

High-Level Synthesis Design

- Synthesizable C++ code for FPGAs
- Support for Xilinx Vivado HLS and 3rd party HLS tools
- Allows for higher level abstraction than RTL
- Highly optimized C++ code as well as low-level optimizations (individual LUTs, memories, etc.)
- Fast validation using C/C++ testbench
- Easy integration into existing HLS or RTL projects

Timing (Max Clock Frequency)

(examples based on Kintex Ultrascale FPGAs)

2 to 1 Viterbi:	Fmax = 464 MHz
4 to 2 Viterbi:	Fmax = 361 MHz

*Note, Fmax will depend on FPGA device, speed grade, design density and other design factors.

Throughput and Resource Utilization

(examples based on Kintex Ultrascale FPGAs)

Latency:

2 to 1 Viterbi:	Max of 12 cycles	25.9 ns
4 to 2 Viterbi:	Max of 14 cycles	38.8 ns

Throughput

2 to 1 Viterbi:	1 soft-bit per cycle	464 Msps
4 to 2 Viterbi:	2 soft-bits per cycle	722 Msps

Resource Utilization

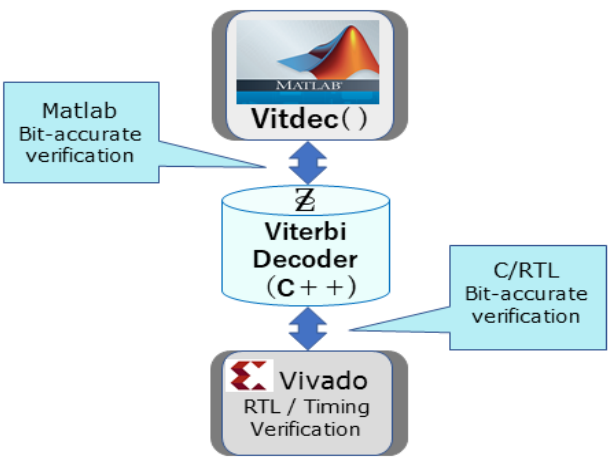
2 to 1 Viterbi:	CLB	LUT	FF	BRAM
Low Fmax, Small area	858	4444	4152	0
High Fmax, More Pipelining	1020	4604	7657	0

4 to 2 Viterbi:	CLB	LUT	FF	BRAM
Low Fmax, Small area	4836	19827	28644	0
High Fmax, More Pipelining	3693	21477	29898	0

*Note, resource utilization will vary depending on the target clock frequency. More pipeline registers will automatically be inserted in order to meet higher frequencies.

Testing and Verification

- Tested in C, RTL simulation and hardware
- Used by customers in a high-performance communications system
- Convolutional encoding testbench included
- Bit accurate with Matlab's vitdec



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